

Computation of parasitic capacitances of an IC cell in accounting for lithography effect

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Abstract

Today's sub-wavelength IC design needs the reticle enhancement technology (RET) such as optical proximity correction (OPC) to correct optical distortion due to photolithography effect. However the difference between the drawn layout and the actual print image persists. To accurately predict the interconnect parasitics such as resistances and capacitances, the impact of optical distortion needs to be considered. This paper presents the computation of parasitic capacitances of an IC logical cell in accounting for optical distortion by using a three dimensional field solver. Starting from the drawn layout of the logical cell, we perform an optical proximity correction by using a model-based technique (Calibre™ OPCpro) to compensate the distortion due to the optical proximity effect. Then we use Calibre™ Printimage tool to obtain the simulated print image. The parasitic capacitances are calculated on both the drawn layout and the post-OPC print image by solving the three dimensional electrostatic field. The results show a significant impact of lithography print image on parasitic capacitances. The present study offers a better understanding of the impact of optical effect on the accuracy of parasitic capacitances and provides an overview for further optical effect modeling and post OPC extraction.